

Update Search

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	2147	(retard\$5 stop\$4 prevent\$5 reduc\$5 eliminat\$5 block\$4) with diffus\$5 same ((carbon C) with (oxygen "O. sub.2"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 15:41
L6	3	5 and ((iodine "I.sub.2") with alcohol\$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 15:58
L7	64	5 and (ALD\$1 (atomic adj layer\$2 adj deposit\$5))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 15:08
L16	17714	(retard\$5 stop\$4 prevent\$5 reduc\$5 eliminat\$5 block\$4) with diffus\$5 with (dopant\$1 impurit\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 15:57
L17	177	16 same ((carbon C) with (oxygen "O. sub.2"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 15:56
L19	94	17 same (heat\$3 anneal\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 15:57

Interference Search

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L10	2	(mono adj layer\$1) with (carbon C) with (oxygen "O.sub.2")	US-PGPUB	OR	OFF	2006/01/07 15:15


PALM INTRANET

 Day : Saturday
 Date: 1/7/2006
 Time: 15:22:48
Inventor Name Search Result

Your Search was:

Last Name = CHAN

First Name = KEVIN K.

Application#	Patent#	Status	Date Filed	Title	Inventor Name
06923977	4689111	150	10/28/1986	PROCESS FOR PROMOTING THE INTERLAMINATE ADHESION OF POLYMERIC MATERIALS TO METAL SURFACES	CHAN, KEVIN K.
07049254	4797178	150	05/13/1987	PLASMA ETCH ENHANCEMENT WITH LARGE MASS INERT GAS	CHAN, KEVIN K.
07413357	5190792	150	09/27/1989	HIGH-THROUGHPUT, LOW-TEMPERATURE PROCESS FOR DEPOSITING OXIDES	CHAN, KEVIN K.
07435216	4978421	250	11/13/1989	MONOLITHIC SILICON MEMBRANE DEVICE FABRICATION PROCESS	CHAN, KEVIN K.
07593141	5133986	150	10/05/1990	PLASMA ENHANCED CHEMICAL VAPOR PROCESSING SYSTEM USING HOLLOW CATHODE EFFECT	CHAN, KEVIN K.
07984816	Not Issued	161	12/03/1992	HIGH-THROUGHPUT, LOW-TEMPERATURE PROCESS FOR DEPOSITING OXIDES	CHAN, KEVIN K.
08240060	5427630	150	05/09/1994	MASK MATERIAL FOR LOW TEMPERATURE SELECTIVE GROWTH OF SILICON OR SILICON ALLOYS	CHAN, KEVIN K.
08247170	5451535	250	05/20/1994	METHOD FOR MANUFACTURING A MEMORY CELL	CHAN, KEVIN K.
08390132	5565031	150	02/17/1995	METHOD FOR LOW TEMPERATURE SELECTIVE GROWTH OF SILICON OR SILICON ALLOYS	CHAN, KEVIN K.
08469650	5595600	150	06/06/1995	LOW TEMPERATURE SELECTIVE GROWTH OF SILICON OR SILICON ALLOYS	CHAN, KEVIN K.
08587029	5634973	250	01/16/1996	LOW TEMPERATURE SELECTIVE GROWTH OF SILICON OR SILICON ALLOYS	CHAN, KEVIN K.
08683329	Not	161	07/18/1996	SCALABLE MOS FIELD EFFECT	CHAN, KEVIN K.

	Issued			TRANSISTOR	
09207353	6350321	150	12/08/1998	UHV HORIZONTAL HOT WALL CLUSTER CVD/GROWTH DESIGN	CHAN, KEVIN K.
09272297	6365465	150	03/19/1999	SELF-ALIGNED DOUBLE-GATE MOSFET BY SELECTIVE EPITAXY AND SILICON WAFER BONDING TECHNIQUES	CHAN, KEVIN K.
09312943	6255200	150	05/17/1999	POLYSILICON STRUCTURE AND PROCESS FOR IMPROVING CMOS DEVICE PERFORMANCE	CHAN, KEVIN K.
09337550	6238737	150	06/22/1999	METHOD FOR PROTECTING REFRACTORY METAL THIN FILM REQUIRING HIGH TEMPERATURE PROCESSING IN AN OXIDIZING ATMOSPHERE AND STRUCTURE FORMED THEREBY	CHAN, KEVIN K.

Inventor Search Completed: No Records to Display.

Search Another: Inventor	Last Name	First Name	<input type="button" value="Search"/>
	<input type="text" value="chan"/>	<input type="text" value="kevin k."/>	

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PALM INTRANET

Day : Saturday
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Inventor Name Search Result

Your Search was:

Last Name = CHEN

First Name = HUAJIE

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10127196	6762469	150	04/19/2002	HIGH PERFORMANCE CMOS DEVICE STRUCTURE WITH MID-GAP METAL GATE	CHEN, HUAJIE
10249563	6780695	150	04/18/2003	BICMOS INTEGRATION SCHEME WITH RAISED EXTRINSIC BASE	CHEN, HUAJIE
10250100	6777302	150	06/04/2003	NITRIDE PEDESTAL FOR RAISED EXTRINSIC BASE HBT PROCESS	CHEN, HUAJIE
10250181	6749684	150	06/10/2003	METHOD FOR IMPROVING CVD FILM QUALITY UTILIZING POLYSILICON GETTERER	CHEN, HUAJIE
10345469	6844225	150	01/15/2003	SELF-ALIGNED MASK FORMED UTILIZING DIFFERENTIAL OXIDATION RATES OF MATERIALS	CHEN, HUAJIE
10448954	Not Issued	93	05/30/2003	SIGE LATTICE ENGINEERING USING A COMBINATION OF OXIDATION, THINNING AND EPITAXIAL REGROWTH	CHEN, HUAJIE
10604607	6891192	150	08/04/2003	STRUCTURE AND METHOD OF MAKING STRAINED SEMICONDUCTOR CMOS TRANSISTORS HAVING LATTICE-MISMATCHED SEMICONDUCTOR REGIONS UNDERLYING SOURCE AND DRAIN REGIONS	CHEN, HUAJIE
10604907	6924517	150	08/26/2003	THIN CHANNEL FET WITH RECESSED SOURCE/DRAINS AND EXTENSIONS	CHEN, HUAJIE
10605134	6906360	150	09/10/2003	STRUCTURE AND METHOD OF MAKING STRAINED CHANNEL CMOS TRANSISTORS HAVING LATTICE-MISMATCHED EPITAXIAL EXTENSION AND SOURCE AND DRAIN REGIONS	CHEN, HUAJIE
10610612	Not	30	07/01/2003	Defect reduction by oxidation of silicon	CHEN, HUAJIE

	Issued				
<u>10654232</u>	<u>6989058</u>	150	09/03/2003	USE OF THIN SOI TO INHIBIT RELAXATION OF SIGE LAYERS	CHEN, HUAJIE
<u>10689506</u>	Not Issued	71	10/20/2003	High performance stress-enhanced MOSFETs using Si:C and SiGe epitaxial source/drain and method of manufacture	CHEN, HUAJIE
<u>10708378</u>	Not Issued	80	02/27/2004	HYBRID SOI/BULK SEMICONDUCTOR TRANSISTORS	CHEN, HUAJIE
<u>10709239</u>	Not Issued	71	04/23/2004	STRUCTURES AND METHODS FOR MANUFACTURING OF DISLOCATION FREE STRESSED CHANNELS IN BULK SILICON AND SOI CMOS DEVICES BY GATE STRESS ENGINEERING WITH SiGe AND/OR Si:C	CHEN, HUAJIE
<u>10710255</u>	<u>6893936</u>	150	06/29/2004	METHOD OF FORMING STRAINED SI/SIGE ON INSULATOR WITH SILICON GERMANIUM BUFFER	CHEN, HUAJIE
<u>10710737</u>	Not Issued	71	07/30/2004	CHEMICAL TREATMENT TO RETARD DIFFUSION IN A SEMICONDUCTOR OVERLAYER	CHEN, HUAJIE
<u>10710826</u>	Not Issued	41	08/05/2004	METHOD OF FORMING STRAINED SILICON MATERIALS WITH IMPROVED THERMAL CONDUCTIVITY	CHEN, HUAJIE
<u>10711637</u>	Not Issued	41	09/29/2004	STRUCTURE AND METHOD FOR MAKING STRAINED CHANNEL FIELD EFFECT TRANSISTOR USING SACRIFICIAL SPACER	CHEN, HUAJIE
<u>10711899</u>	Not Issued	80	10/12/2004	ULTRA SHALLOW JUNCTION FORMATION BY EPITAXIAL INTERFACE LIMITED DIFFUSION	CHEN, HUAJIE
<u>10728519</u>	<u>6972247</u>	150	12/05/2003	METHOD OF FABRICATING STRAINED SI SOI WAFERS	CHEN, HUAJIE
<u>10751207</u>	Not Issued	61	01/02/2004	Method of preventing surface roughening during hydrogen pre-bake of SiGe substrates using chlorine containing gases	CHEN, HUAJIE
<u>10751208</u>	<u>6958286</u>	150	01/02/2004	METHOD OF PREVENTING SURFACE ROUGHENING DURING HYDROGEN PREBAKE OF SIGE SUBSTRATES	CHEN, HUAJIE
<u>10795672</u>	<u>6916698</u>	150	03/08/2004	HIGH PERFORMANCE CMOS DEVICE STRUCTURE WITH MID-GAP METAL GATE	CHEN, HUAJIE
<u>10818572</u>	Not Issued	41	04/06/2004	Method of forming high-quality relaxed SiGe alloy layers on bulk Si substrates	CHEN, HUAJIE

10855915	Not Issued	61	05/27/2004	High-quality SGOI by annealing near the alloy melting point	CHEN, HUAJIE
10890765	Not Issued	41	07/14/2004	Ion implantation for suppression of defects in annealed SiGe layers	CHEN, HUAJIE
10905595	Not Issued	30	01/12/2005	LOW CONCENTRATION SiGe BUFFER DURING STRAINED Si GROWTH OF SSGOI MATERIAL FOR DOPANT DIFFUSION CONTROL AND DEFECT REDUCTION	CHEN, HUAJIE
10905598	Not Issued	30	01/12/2005	IN SITU DOPED EMBEDDED SIGE EXTENSION AND SOURCE/DRAIN FOR ENHANCED PFET PERFORMANCE	CHEN, HUAJIE
10905978	Not Issued	30	01/28/2005	STRUCTURE AND METHOD FOR MANUFACTURING PLANAR STRAINED Si/SiGe SUBSTRATE WITH MULTIPLE ORIENTATIONS AND DIFFERENT STRESS LEVELS	CHEN, HUAJIE
10908394	Not Issued	30	05/10/2005	EMBEDDED SILICON GERMANIUM USING A DOUBLE BURIED OXIDE SILICON-ON-INSULATOR WAFER	CHEN, HUAJIE
10943048	Not Issued	30	09/16/2004	Buffer layer for selective SiGe growth for uniform nucleation	CHEN, HUAJIE
10969718	Not Issued	30	10/20/2004	Self-aligned mask formed utilizing differential oxidation rates of materials	CHEN, HUAJIE
11037622	Not Issued	30	01/18/2005	Structure and method for manufacturing strained silicon directly-on-insulator substrate with hybrid crystalline orientation and different stress levels	CHEN, HUAJIE
11081271	Not Issued	30	03/16/2005	Method of making strained semiconductor transistors having lattice-mismatched semiconductor regions underlying source and drain regions	CHEN, HUAJIE
11268096	Not Issued	20	11/07/2005	Use of thin SOI to inhibit relaxation of SiGe layers	CHEN, HUAJIE

Inventor Search Completed: No Records to Display.

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	<input type="text" value="Chen"/>	<input type="text" value="Huajie"/>	

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Inventor Name Search Result

Your Search was:

Last Name = HOLT

First Name = JUDSON

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10710245	Not Issued	30	06/29/2004	DOPED NITRIDE FILM, DOPED OXIDE FILM AND OTHER DOPED FILMS	HOLT, JUDSON
10835949	Not Issued	94	04/30/2004	MATERIAL FOR CONTACT ETCH LAYER TO ENHANCE DEVICE PERFORMANCE	HOLT, JUDSON
11253622	Not Issued	20	10/20/2005	Material for contact etch layer to enhance device performance	HOLT, JUDSON
10710736	Not Issued	95	07/30/2004	ULTRA-THIN BODY SUPER-STEEP RETROGRADE WELL (SSRW) FET DEVICES	HOLT, JUDSON R.
10710737	Not Issued	71	07/30/2004	CHEMICAL TREATMENT TO RETARD DIFFUSION IN A SEMICONDUCTOR OVERLAYER	HOLT, JUDSON R.
11029797	Not Issued	30	01/05/2005	Stressed field effect transistors on hybrid orientation substrate	HOLT, JUDSON R.
11088595	Not Issued	30	03/24/2005	High performance field effect transistors on SOI substrate with stress-inducing material as buried insulator and methods	HOLT, JUDSON R.
11161964	Not Issued	30	08/24/2005	METHOD FOR POST-RIE PASSIVATION OF SEMICONDUCTOR SURFACES FOR EPITAXIAL GROWTH	HOLT, JUDSON R.
60732354	Not Issued	20	10/31/2005	Implant damage control by in-situ C doping during SiGe epitaxy for device applications	HOLT, JUDSON ROBERT

Inventor Search Completed: No Records to Display.

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PALM INTRANET

 Day : Saturday
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Inventor Name Search Result

Your Search was:

Last Name = LEE

First Name = WOO-HYEONG

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08871024	Not Issued	161	10/10/1996	FLOATING -GATE MEMORY DEVICE AND PROCESS FOR MAKING SAME	LEE, WOO-HYEONG
09041434	5923056	150	03/12/1998	ELECTRONIC COMONENTS WITH DOPED METAL OXIDE DIELECTRIC MATERIALS AND A PROCESS FOR MAKING ELECTRONIC COMPONENTS WITH DOPED METAL OXIDE DIELECTRIC MATERIALS	LEE, WOO-HYEONG
10684596	Not Issued	121	10/15/2003	Deposition of carbon and nitrogen doped poly silicon films, and retarded boron diffusion and improved poly depletion	LEE, WOO-HYEONG
10707878	Not Issued	41	01/20/2004	Polycrystalline Silicon Layer With Nano-grain Structure and Method of Manufacture	LEE, WOO-HYEONG
10710737	Not Issued	71	07/30/2004	CHEMICAL TREATMENT TO RETARD DIFFUSION IN A SEMICONDUCTOR OVERLAYER	LEE, WOO-HYEONG
10786901	Not Issued	41	02/25/2004	CMOS silicide metal gate integration	LEE, WOO-HYEONG
10905948	Not Issued	30	01/27/2005	TRANSISTOR HAVING HIGH MOBILITY CHANNEL AND METHODS	LEE, WOO-HYEONG
60027612	Not Issued	159	10/10/1996	FLOATING-GATE MEMORY DEVICE AND PROCESS FOR MAKING SAME	LEE, WOO-HYEONG

Inventor Search Completed: No Records to Display.

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Lee
Woo-Hyeong
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 PALM INTRANETDay : Saturday
Date: 1/7/2006
Time: 15:33:54**Inventor Name Search Result**

Your Search was:

Last Name = MITCHELL

First Name = RYAN


Application#	Patent#	Status	Date Filed	Title	Inventor Name
09805380	Not Issued	160	03/13/2001	Method and system for analyzing and planning an inventory	MITCHELL, RYAN J.
09805720	Not Issued	161	03/08/2001	Method and system for analyzing and planning an inventory	MITCHELL, RYAN J.
11038975	Not Issued	30	01/19/2005	Voice-over-internet protocol gateway	MITCHELL, RYAN J.
60654328	Not Issued	20	02/17/2005	VOIP to wireless gateway	MITCHELL, RYAN J.
10674647	Not Issued	30	09/30/2003	Thin buried oxides by low-dose oxygen implantation into modified silicon	MITCHELL, RYAN M.
10710737	Not Issued	71	07/30/2004	CHEMICAL TREATMENT TO RETARD DIFFUSION IN A SEMICONDUCTOR OVERLAYER	MITCHELL, RYAN M.
10710826	Not Issued	41	08/05/2004	METHOD OF FORMING STRAINED SILICON MATERIALS WITH IMPROVED THERMAL CONDUCTIVITY	MITCHELL, RYAN M.

Inventor Search Completed: No Records to Display.

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PALM INTRANET

Day : Saturday
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Inventor Name Search Result

Your Search was:

Last Name = MO

First Name = RENEE

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10249296	6790733	150	03/28/2003	PRESERVING TEOS HARD MASK USING COR FOR RAISED SOURCE-DRAIN INCLUDING REMOVABLE/DISPOSABLE SPACER	MO, RENEE T.
10605311	Not Issued	95	09/22/2003	METHOD FOR AVOIDING OXIDE UNDERCUT DURING PRE-SILICIDE CLEAN FOR THIN SPACER FETS	MO, RENEE T.
10710001	Not Issued	51	06/11/2004	Forming Shallow Trench Isolation Without the Use of CMP	MO, RENEE T.
10710736	Not Issued	95	07/30/2004	ULTRA-THIN BODY SUPER-STEEP RETROGRADE WELL (SSRW) FET DEVICES	MO, RENEE T.
10710737	Not Issued	71	07/30/2004	CHEMICAL TREATMENT TO RETARD DIFFUSION IN A SEMICONDUCTOR OVERLAYER	MO, RENEE T.
10710738	Not Issued	41	07/30/2004	MANUFACTURABLE RECESSED STRAINED RSD STRUCTURE AND PROCESS FOR ADVANCED CMOS	MO, RENEE T.
10905683	Not Issued	30	01/17/2005	NITRIDATION OF STI FILL OXIDE TO PREVENT THE LOSS OF STI FILL OXIDE DURING MANUFACTURING PROCESS	MO, RENEE T.
10907061	Not Issued	30	03/18/2005	CLUSTERED SURFACE PREPARATION FOR SILICIDE AND METAL CONTACTS	MO, RENEE T.
10942303	Not Issued	71	09/16/2004	Method for monitoring lateral encroachment of spacer process on a CD SEM	MO, RENEE T.
11266855	Not Issued	41	11/04/2005	Method for avoiding oxide undercut during pre-silicide clean for thin spacer FETs	MO, RENEE T.
11177246	Not Issued	20	07/07/2005	Positron therapy of inflammation, infection and disease	MOADEL, RENEE M.
60586366	Not	159	07/08/2004	Positron therapy of inflammation, infection	MOADEL, RENEE M.

	Issued			an disease	
10097461	6681508	150	03/14/2002	VISUAL DISPLAY DEVICE	MONTEIRO, RENEE A.
60275738	Not Issued	159	03/14/2001	Color geyser lamp	MONTEIRO, RENEE A.
06841146	Not Issued	161	03/19/1986	BONDING OF ARTICLES TO METALLIZED SUBSTRATES	MOORE, RENEE D.
09204449	6132051	250	12/03/1998	MIRROR ATTACHMENT	MORELL, RENEE
60334324	Not Issued	159	11/29/2001	Methods to inhibit thiol-mediated biocatalysis	MOSI, RENEE
60120618	Not Issued	159	02/18/1999	METALLO-BETA-LACTAMASE INHIBITORS	MOSI, RENEE MARIE

Inventor Search Completed: No Records to Display.

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Inventor Name Search Result

Your Search was:

Last Name = MOCUTA

First Name = DAN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10250181	6749684	150	06/10/2003	METHOD FOR IMPROVING CVD FILM QUALITY UTILIZING POLYSILICON GETTERER	MOCUTA, DAN
10127196	6762469	150	04/19/2002	HIGH PERFORMANCE CMOS DEVICE STRUCTURE WITH MID-GAP METAL GATE	MOCUTA, DAN M.
10707840	Not Issued	41	01/16/2004	Protecting Silicon Germanium Sidewall with Silicon for Strained Silicon/Silicon Germanium MOSFETs	MOCUTA, DAN M.
10710737	Not Issued	71	07/30/2004	CHEMICAL TREATMENT TO RETARD DIFFUSION IN A SEMICONDUCTOR OVERLAYER	MOCUTA, DAN M.
10751207	Not Issued	61	01/02/2004	Method of preventing surface roughening during hydrogen pre-bake of SiGe substrates using chlorine containing gases	MOCUTA, DAN M.
10751208	6958286	150	01/02/2004	METHOD OF PREVENTING SURFACE ROUGHENING DURING HYDROGEN PREBAKE OF SIGE SUBSTRATES	MOCUTA, DAN M.
10795672	6916698	150	03/08/2004	HIGH PERFORMANCE CMOS DEVICE STRUCTURE WITH MID-GAP METAL GATE	MOCUTA, DAN M.
10954838	Not Issued	30	09/30/2004	Structure and method for manufacturing MOSFET with super-steep retrograded island	MOCUTA, DAN M.

Inventor Search Completed: No Records to Display.

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PALM INTRANET

 Day : Saturday
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Inventor Name Search Result

Your Search was:

Last Name = RAUSCH

First Name = WERNER

Application#	Patent#	Status	Date Filed	Title	Inventor Name
06124504	4265677	150	02/25/1980	PHOSPHATIZING PRIOR TO CATHODIC ELECTROPAINTING	RAUSCH, WERNER
06258171	Not Issued	161	04/27/1981	PHOSPHATIZING	RAUSCH, WERNER
06337916	4389260	150	01/08/1982	COMPOSITION AND PROCESS FOR THE PHOSPHATISING OF METALS	RAUSCH, WERNER
06373475	4419199	150	04/30/1982	PROCESS FOR PHOSPHATIZING METALS	RAUSCH, WERNER
06593985	Not Issued	161	03/27/1984	PROCESS AND COMPOSITION FOR PHOSPHATING METAL SURFACES	RAUSCH, WERNER
06600587	4559087	250	04/17/1984	PROCESS FOR PHOSPHATING METALS	RAUSCH, WERNER
06601184	Not Issued	161	04/17/1984	PROTECTING METALS FROM CORROSION	RAUSCH, WERNER
06653504	4547269	150	09/21/1984	METHOD OF ELECTRODEPOSITING ZINC ON STEEL PRIOR TO PHOSPHATING	RAUSCH, WERNER
06708463	4637838	250	03/05/1985	PROCESS FOR PHOSPHATING METALS	RAUSCH, WERNER
07092951	4849031	150	09/04/1987	PROCESS OF PRODUCING PHOSPHATE COATINGS ON METAL SURFACES	RAUSCH, WERNER
07106165	4867853	150	10/07/1987	PROCESS OF PRODUCING PHOSPHATE COATINGS	RAUSCH, WERNER
07156777	Not Issued	166	02/17/1988	PROCESS OF PREPARING WORKPIECES OF ALUMINUM OR ALLOYS THEREOF FOR BEING PAINTED	RAUSCH, WERNER
07178124	Not Issued	166	04/06/1988	PROCESS OF PROSPHATING BEFORE ELECTROIMMERSION PAINTING	RAUSCH, WERNER
07230767	Not Issued	161	08/10/1988	PROCESS FOR PHOSPHATING METAL	RAUSCH, WERNER

<u>07259158</u>	Not Issued	161	10/18/1988	PROCESS OF FORMING PHOSPHATE COATINGS	RAUSCH, WERNER
<u>07305214</u>	<u>4950339</u>	250	02/01/1989	PROCESS OF FORMING PHOSPHATE COATINGS ON METALS	RAUSCH, WERNER
<u>07369743</u>	<u>5024707</u>	150	06/22/1989	PROCESS OF DECREASING THE INCRUSTATION IN PHOSPHATING PLANTS	RAUSCH, WERNER
<u>07395478</u>	Not Issued	166	08/18/1989	PHOSPHATING PROCESS	RAUSCH, WERNER
<u>07398185</u>	Not Issued	166	08/24/1989	METHOD OF APPLYING PHOSPHATE COATINGS	RAUSCH, WERNER
<u>07428013</u>	Not Issued	166	10/26/1989	PROCESS OF PHOSPHATING BEFORE ELECTROIMMERSION PAINTING	RAUSCH, WERNER
<u>07456191</u>	Not Issued	161	12/15/1989	PROCESS OF PREPARING WORKPIECES OF ALUMINUM OR ALLOYS THEREOF FOR BEING PAINTED	RAUSCH, WERNER
<u>07484730</u>	Not Issued	164	02/23/1990	PROCESS FOR A PASSIVATING POSTRINSING OF PHOSPHATE LAYERS	RAUSCH, WERNER
<u>07570350</u>	<u>5203930</u>	150	08/21/1990	PROCESS OF FORMING PHOSPHATE COATINGS ON METAL SURFACES	RAUSCH, WERNER
<u>07570421</u>	Not Issued	166	08/21/1990	PROCESS OF PRODUCING PHOSPHATE COATINGS ON METALS	RAUSCH, WERNER
<u>07629076</u>	<u>5236565</u>	250	12/17/1990	PROCESS OF PHOSPHATING BEFORE ELECTROIMMERSION PAINTING	RAUSCH, WERNER
<u>07645159</u>	Not Issued	166	01/24/1991	COMPOSITION AND PROCESS FOR A PASSIVATING POSTRINSING OF CONVERSION LAYERS	RAUSCH, WERNER
<u>07683106</u>	<u>5152849</u>	150	04/10/1991	PHOSPHATING PROCESS	RAUSCH, WERNER
<u>07691129</u>	Not Issued	166	04/24/1991	PROCESS FOR PHOSPHATING METAL SURFACES	RAUSCH, WERNER
<u>07759840</u>	Not Issued	161	09/13/1991	METHOD OF APPLYING PHOSPHATE COATINGS	RAUSCH, WERNER
<u>07793220</u>	Not Issued	163	11/07/1991	PROCESS FOR PRODUCING PHOSPHATE COATINGS ON METALS	RAUSCH, WERNER
<u>07977668</u>	Not Issued	161	11/18/1992	METHOD OF APPLYING PHOSPHATE COATINGS	RAUSCH, WERNER
<u>07978193</u>	<u>5294266</u>	150	11/18/1992	PROCESS FOR A PASSIVATING POSTRINSING OF CONVERSION LAYERS	RAUSCH, WERNER

<u>08797904</u>	<u>6022766</u>	150	02/10/1997	SEMICONDUCTOR STRUCTURE INCORPORATING THIN FILM TRANSISTORS, AND METHODS FOR ITS MANUFACTURE	RAUSCH, WERNER
<u>09231615</u>	<u>6188122</u>	150	01/14/1999	BURIED CAPACITOR FOR SILICON-ON-INSULATOR STRUCTURE	RAUSCH, WERNER
<u>09239327</u>	<u>6521947</u>	150	01/28/1999	METHOD OF INTEGRATING SUBSTRATE CONTACT ON SOI WAFERS WITH STI PROCESS	RAUSCH, WERNER
<u>09377331</u>	<u>6686629</u>	150	08/18/1999	SOI MOSFETS EXHIBITING REDUCED FLOATING-BODY EFFECTS	RAUSCH, WERNER
<u>09707305</u>	<u>6337253</u>	150	11/07/2000	Process of making buried capacitor for silicon-on-insulator structure	RAUSCH, WERNER
<u>09717971</u>	<u>6303450</u>	150	11/21/2000	Novel CMOS device structures and method of making same	RAUSCH, WERNER
<u>09770788</u>	<u>6713791</u>	150	01/26/2001	T-RAM ARRAY HAVING A PLANAR CELL STRUCTURE AND METHOD FOR FABRICATING THE SAME	RAUSCH, WERNER
<u>09875842</u>	<u>6432777</u>	150	06/06/2001	METHOD FOR INCREASING THE EFFECTIVE WELL DOPING IN A MOSFET AS THE GATE LENGTH DECREASES	RAUSCH, WERNER
<u>10713447</u>	Not Issued	71	11/14/2003	CMOS well structure and method of forming the same	RAUSCH, WERNER
<u>10732277</u>	Not Issued	41	12/11/2003	SOI MOSFETS exhibiting reduced floating-body effects	RAUSCH, WERNER
<u>11164515</u>	Not Issued	19	01/01/0001	CMOS CIRCUITS INCORPORATING PASSIVE ELEMENTS OF LOW CONTACT RESISTANCE, AND METHODS OF FORMING SAME	RAUSCH, WERNER
<u>09547893</u>	<u>6624459</u>	150	04/12/2000	SILICON ON INSULATOR FIELD EFFECT TRANSISTOR HAVING SHARED BODY CONTACT	RAUSCH, WERNER A.
<u>09589719</u>	<u>6429482</u>	150	06/08/2000	HALO-FREE NON-RECTIFYING CONTACT ON CHIP WITH HALO SOURCE/DRAIN DIFFUSION	RAUSCH, WERNER A.
<u>10064305</u>	<u>6750109</u>	150	07/01/2002	HALO-FREE NON-RECTIFYING CONTACT ON CHIP WITH HALO SOURCE/DRAIN DIFFUSION	RAUSCH, WERNER A.
<u>10250047</u>	<u>6887798</u>	150	05/30/2003	STI STRESS MODIFICATION BY NITROGEN PLASMA TREATMENT FOR IMPROVING PERFORMANCE IN SMALL WIDTH DEVICES	RAUSCH, WERNER A.
<u>10453080</u>	<u>6930030</u>	150	06/03/2003	METHOD OF FORMING AN ELECTRONIC DEVICE ON A RECESS	RAUSCH, WERNER A.

				IN THE SURFACE OF A THIN FILM OF SILICON ETCHED TO A PRECISE THICKNESS	
10460717	6815282	150	06/12/2003	SILICON ON INSULATOR FIELD EFFECT TRANSISTOR HAVING SHARED BODY CONTACT	RAUSCH, WERNER A.
10605100	Not Issued	71	09/09/2003	A RAISED SOURCE DRAIN MOSFET WITH NOTCH FORMED ON TOP OF GATE STRUCTURE FILLED WITH A DIELECTRIC PLUG	RAUSCH, WERNER A.

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Inventor Name Search Result

Your Search was:

Last Name = RONSHEIM

First Name = PAUL

Application#	Patent#	Status	Date Filed	Title	Inventor Name
07912945	Not Issued	161	07/13/1992	HETEROJUNCTION BIPOLAR TRANSISTOR WITH SELF-ALIGNED RETROGRADE EMITTER PROFILE	RONSHEIM, PAUL
08346209	5656514	150	11/22/1994	METHOD OF MAKING HETEROJUNCTION BIPOLAR TRANSISTOR WITH SELF-ALIGNED RETROGRADE EMITTER PROFILE	RONSHEIM, PAUL
10250181	6749684	150	06/10/2003	METHOD FOR IMPROVING CVD FILM QUALITY UTILIZING POLYSILICON GETTERER	RONSHEIM, PAUL
09559880	6399434	150	04/26/2000	DOPED STRUCTURES CONTAINING DIFFUSION BARRIERS	RONSHEIM, PAUL A.
09734754	6509241	150	12/12/2000	PROCESS FOR FABRICATING AN MOS DEVICE HAVING HIGHLY-LOCALIZED HALO REGIONS	RONSHEIM, PAUL A.
09866397	Not Issued	161	05/25/2001	Reducing threshold voltage roll-up/roll-off effect for MOSFETS	RONSHEIM, PAUL A.
09875072	6387782	150	06/06/2001	PROCESS OF FORMING AN ULTRA-SHALLOW JUNCTION DOPANT LAYER HAVING A PEAK CONCENTRATION WITHIN A DIELECTRIC LAYER	RONSHEIM, PAUL A.
09924014	6635517	150	08/07/2001	USE OF DISPOSABLE SPACER TO INTRODUCE GETTERING IN SOI LAYER	RONSHEIM, PAUL A.
10710737	Not Issued	71	07/30/2004	CHEMICAL TREATMENT TO RETARD DIFFUSION IN A SEMICONDUCTOR OVERLAYER	RONSHEIM, PAUL A.
10762279	Not Issued	160	01/23/2004	Method for manufacturing a MOSFET device	RONSHEIM, PAUL A.
07652339	5385850	150	02/07/1991	METHOD OF FORMING A DOPED REGION IN A SEMICONDUCTOR SUBSTRATE UTILIZING A SACRIFICIAL EPITAXIAL SILICON	RONSHEIM, PAUL A.


				LAYER	
07710498	5194397	150	06/05/1991	METHOD FOR CONTROLLING INTERFACIAL OXIDE AT A POLYCRYSTALLINE/MONOCRYSTALLINE SILICON INTERFACE	RONSCHEIM, PAUL A.
08457084	5616513	250	06/01/1995	SHALLOW TRENCH ISOLATION WITH SELF ALIGNED PSG LAYER	RONSCHEIM, PAUL A.
09153986	6114257	150	09/16/1998	PROCESS FOR MODIFIED OXIDATION OF A SEMICONDUCTOR SUBSTRATE USING CHLORINE PLASMA	RONSCHEIM, PAUL A.
09213674	6194736	150	12/17/1998	QUANTUM CONDUCTIVE RECRYSTALLIZATION BARRIER LAYERS	RONSCHEIM, PAUL A.
09458530	6329704	150	12/09/1999	ULTRA-SHALLOW JUNCTION DOPANT LAYER HAVING A PEAK CONCENTRATION WITHIN A DIELECTRIC LAYER	RONSCHEIM, PAUL A.
09968793	Not Issued	161	10/03/2001	Method for fabricating different gate oxide thickness within the same chip	RONSCHEIM, PAUL ANDREW
09090735	Not Issued	161	06/04/1998	METHOD FOR FABRICATING DIFFERENT GATE OXIDE THICKNESSES WITHIN THE SAME CHIP	RONSCHEIM, PAUL ANDREW
09231617	6335262	150	01/14/1999	METHOD FOR FABRICATING DIFFERENT GATE OXIDE THICKNESSES WITHIN THE SAME CHIP	RONSCHEIM, PAUL ANDREW

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Your Search was:

Last Name = UTOMO

First Name = HENRY

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10710737	Not Issued	71	07/30/2004	CHEMICAL TREATMENT TO RETARD DIFFUSION IN A SEMICONDUCTOR OVERLAYER	UTOMO, HENRY K.
10711637	Not Issued	41	09/29/2004	STRUCTURE AND METHOD FOR MAKING STRAINED CHANNEL FIELD EFFECT TRANSISTOR USING SACRIFICIAL SPACER	UTOMO, HENRY K.
10905598	Not Issued	30	01/12/2005	IN SITU DOPED EMBEDDED SIGE EXTENSION AND SOURCE/DRAIN FOR ENHANCED PFET PERFORMANCE	UTOMO, HENRY K.
10908394	Not Issued	30	05/10/2005	EMBEDDED SILICON GERMANIUM USING A DOUBLE BURIED OXIDE SILICON-ON-INSULATOR WAFER	UTOMO, HENRY K.
11163871	Not Issued	20	11/02/2005	LOW MODULUS SPACERS FOR CHANNEL STRESS ENHANCEMENT	UTOMO, HENRY K.

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